MURANG'A UNIVERSITY OF TECHNOLOGY

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF _____

UNIVERSITY ORDINARY EXAMINATION

2023/2024 ACADEMIC YEAR

----------YEAR **SECOND** SEMESTER EXAMINATION FOR BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EET 214: BASIC CIRCUIT DESIGN

DURATION: 2 HOURS

INSTRUCTIONS TO CANDIDATES:

1. Answer Question one and any other two questions.
2. Mobile phones are not allowed in the examination room.
3. You are not allowed to write on this examination question paper.

SECTION A: ANSWER ALL QUESTIONS IN THIS SECTION

QUESTION ONE (30 MARKS)

1 a) Define

i. Sequential circuits

ii. Combinational circuits (4marks)

b) Differentiate between Dynamic and static RAM (2marks)

c) Convert i) 1001.01_2 into decimal

ii) $5C7_H$ to decimal

iii) 2598.675_{10} to Hexadecimal (6marks)

d) List three characteristics of an effective memory (3marks)

e) Using a diagram draw the truth table of an AND gate (3marks)

f) State DeMorgans theorem (3marks)

g) Simplify the following function

F(x,y,_____) = xy + _____+ y_____ (5marks)

h) Realize a 5kflip flop using D flipflop (4marks)

SECTION TWO: ANSWER ANY TWO QUESTIONS

QUESTION TWO (20 MARKS)

a) Express the Boolean function F=A + B'C as the sum of miniterms (7marks)

b) Using a well labelled diagram, explain the Von Neumann architecture (13marks)

QUESTION THREE (20 MARKS)

a) Using NAND gates design an SR flip flop and generate a truth fable, characteristic and an excitation table. (12marks)

b) From the SR flip flop designed abode, show how a JK flip flop designed above, show how a JK flip flop can be obtained. Generate its truth table, characteristic and excitation table (8marks)

QUESTION FOUR (20 MARKS)

a) Using a well labelled diagram, discuss the memory hierarchy (13marks)

b) Using a truth table, prove that $AB + \bar{A}C + BC + AB + \bar{A}C$ (7marks)