MURANG'A UNIVERSITY OF TECHNOLOGY

SCHOOL OF ENGINEERING TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

UNIVERSITY ORDINARY EXAMINATION

2023/2024 ACADEMIC YEAR

…….. YEAR **SECOND** SEMESTER EXAMINATION FOR, BACHELOR OF SCIENCE IN ……..

EES 312– COMMUNICATION SYSTEM 11

DURATION: 2 HOURS

Instructions to candidates:

1. Answer question One and Any Other Two questions.
2. Mobile phones are not allowed in the examination room.
3. You are not allowed to write on this examination question paper.

SECTION A: ANSWER ALL QUESTIONS IN THIS SECTION

QUESTION ONE (30 MARKS)

a) Define the following terminologies (6marks)
   i) Jamming margin
   ii) Processing gain
   iii) Attenuation
   iv) Bandwidth
   v) Throughput
   vi) Baudrate

b) Using equivalent diagrams discuss UART transmission (5marks)

c) Explain using a schematic diagram the operation of non-coherent FSK demodulator (5marks)

d) State four problems associated with communication channels (4marks)

e) In DSSS Communication system the following parametors are provided;

   Data sequence bit duration Tb = 4.095ms

   PN chip duration Tb = $1x10^{-6sec}$

   ---------- = 10 for average probability of error less than 10^{-5}

Calculate the processing Gain, jamming margin and the numver of shift registers (5marks)

f) Determine (a) the peak frequency deviation,(b) minimum bandwith and (c) baud for binary FSK signal with f_m = 49KHZ, f_s =SIKH_z and f_b = 2kbps (5marks)

SECTION B – ANSWER ANY TWO QUESTIONS IN THIS SECTION

QUESTION TWO (20 MARKS)

a) A PN sequence is generated using a feedback shift register of length 4 and outputs taken from shift register 4 and 1 respectively. Find the generated output sequence if the initial contents of the shift register are (1011). If the chip rate is 10^7 chips/scc. Calculate the chip duration, the length of the PN sequence and the period of the output sequence. Draw the schematic diagram of the arrangement and the NRZ waveform of the generated output sequence (8marks)

b) Draw the diagram of the frequency synthesizer and explain its function (4marks)

c) The FH/MFSK signal has the following parameters

   Number of bits per MFSK signal k =2

   Number of MFSK tones, M = 2^k = 4

   Length of PN sequence per hop, K = 2

   Total number of frequency hop 2^k = 4

Assume binary data sequence 01110011110110000001 and the PN sequence to be 0011011000. Determine the following

1. Draw the variation of the frequency of FH/MFSK signal for a given PN sequence. Assume that the carrier hops for every two MFSK symbols (5marks)
2. Sketch the variation dehopped frequency with time (3marks)

QUESTION THREE (20 MARKS)

a) State the difference between parallel and serial communication (3marks)
b) Draw a simplified block diagram for a digital radio system (3marks)
c) For a QPSK the following parameters are provided determine (6marks)
   i) Carrier power in dBm
   ii) Noise power in dBm
   iii) Noise power density in dBm
   iv) Energy per bit Dbj
   v) Carrier to noise power ratio in dB
   vi) ----------
d) Draw the schematic diagram of a balanced ring modulator and explain its two modes of operation of logic 1 and logic 0 (8marks)

QUESTION FOUR (20 MARKS)

a) Derive an expression for signal to quantization noise power ratio for delta modulation. Assume that no slope overload distortion exists (10marks)
b) A DM system is designed to operate at 3 times the Nyquist rate for a signal with 3KHZ bandwidth. The quantizing step size is 250mV.
   i) Determine the maximum amplitude of a 1KHZ input sinusoid for which delta modulator does not show slope overload.
   ii) Determine the post filtered output SNR for the signal of part (i) (10marks)