MURANG'A UNIVERSITY OF TECHNOLOGY

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

UNIVERSITY ORDINARY EXAMINATION

2020/2021 ACADEMIC YEAR
THIRD YEAR **SECOND** SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF
TECHNOLOGY IN ELECTRICAL AND ELECTRONIC ENGINEERING
UNIT CODE: EET 310
UNIT NAME: DIGITAL CIRCUIT DESIGN

DURATION: 2 HOURS

Instructions to candidates:

1. Answer question One and any Other Two questions.
2. Mobile phones are not allowed in the examination room.
3. You are not allowed to write on this examination question paper.

SECTION A: ANSWER ALL QUESTIONS IN THIS SECTION

QUESTION ONE (30 MARKS)

(a) (i) Derive a table that converts a 3-bit Gray code $G_2G_1G_o$ into an equivalent 3-bit binary sequence $B_2B_1B_o$ (2 marks)

(ii) Using basic logic gates, design a circuit that could be employed in the conversion of a 3 bit sequence $G_2G_1G_o$ into a 3 bit binary sequence $B_2B_1B_o$. Use a minimum number of logic gates. (6 Marks)

(b) A 4-bit serial shift register is to operate in the following modes.

Mode1 : This allows a serial input/serial output of data with every clock pulse. The data are shifted from left to right

Mode 0: This allows a serial input /serial output of data with every clock pulse. The data are shifted from right to left.

Design the register using D-flip-flops. (8 marks)

(c) A logic circuit has 3 inputs, A, B and C. It has a single output Y. The circuit behaviour is given in the truth table.

Inputs			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Design an implementation of the circuit at component level using CMOS logic. A minimum number of transistors are to be used. (8 marks)

(d) Give a brief discussion of the following 3 types of nose sources common in CMOS circuits. (6 marks)

(i) Johnson noise
(ii) Flicker noise
(iii) Shot noise

SECTION B – ANSWER ANY TWO QUESTIONS IN THIS SECTION

QUESTION TWO (20 MARKS)

(a) An odd parity system has 3 message $m_2m_1m_o$ and one parity check bit p. The whole sequence is $m_2m_1m_op$. Design a detector circuit that could be used at the receiver-end to detect odd parity. The detector should have an output line Y that goes high if the parity is odd otherwise remains low.
Design the circuit with a minimum number of logic gates. (8 marks)

(b) A digital system is given in Fig Q2 (b) attached. Analysed the circuit and obtain the state diagram. (8 marks)

(c) Using T flip-flops, give the design of a 3 –bit Ripple counter. (4 marks)

QUESTION THREE (20 MARKS)

(a) Using a 4-bit arithmetic adder 1C, it is required to implement a subtractor circuit. Let the two 4 –bit inputs be:

$A = A_3A_2A_1A_o$
$B = B_3B_3B_1B_o$

The output is the 4-bit sequence $S = S_3\ S_2\ S_1S_o$ where S =A minus B.
Assume that $A \geq B$
Design the circuit and show all the steps in the procedure. (7 marks)

(b) A digital system has the state diagram given in Fig Q 3 (b) attached. Design the circuit using SR flip flops and a binary decoder amongst other logic components. (8 marks)

(c) Show how a 3-input OR gate could be realized in NMOS technology. A minimum number of components are to be used. (5 marks)

QUESTION FOUR (20 MARKS)

(a) A three-bit Johnson counter is expected to repeat every 10mSec. Determine a suitable clock speed. (3 marks)

(b) A 2 –bit logic multiplier gives the product of two binary sequences A_1A_0 and B_1B_o. Design a suitable circuit using combinational logic components of your choice. Assume that the sequences are available in parallel. (10 marks)

(c) It is required to compare the magnitude of two 4- bit sequences:

$A = A_3A_2A_1\ A_0$
$B = B_3B_2\ B_1B_o$

The output is a 3-bit wide bus $Y_2Y_1Y_o$. If A >B then Y_2 =1, Y_1 =0 and Y_o = 0
And if A = B then $Y_2 = 0\ Y_1 = 1\ Y_o = 0$
and if A<B then $Y_2 = 0\ Y_1 = 0\ Y_o = 1$
Design the circuit using a pair of 2-bit magnitude comparators. (7 marks)